

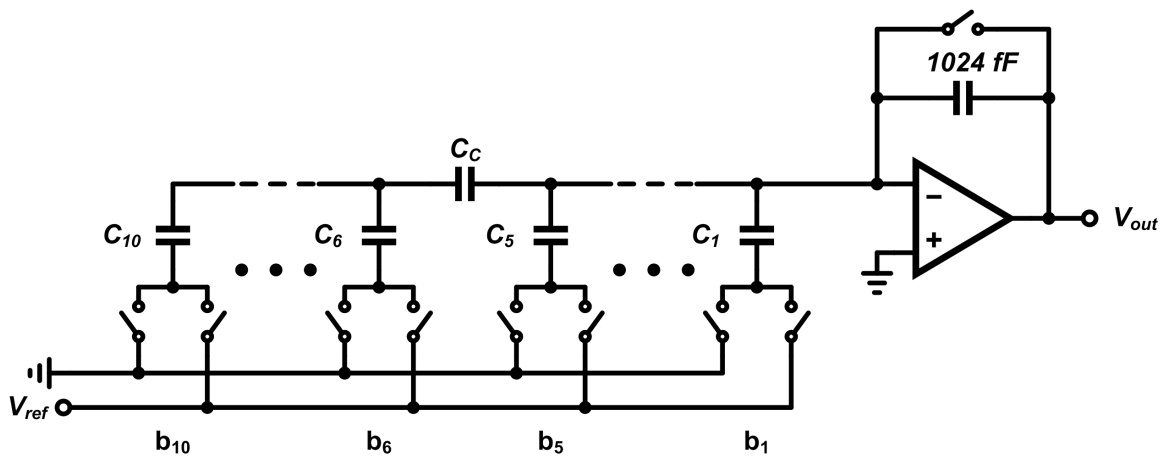
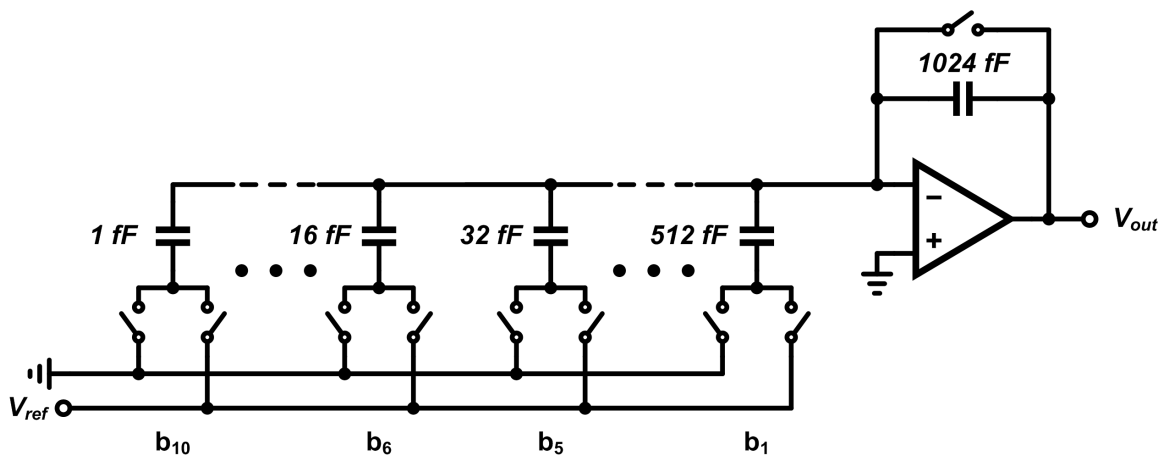
ECE 627

Spring 2011

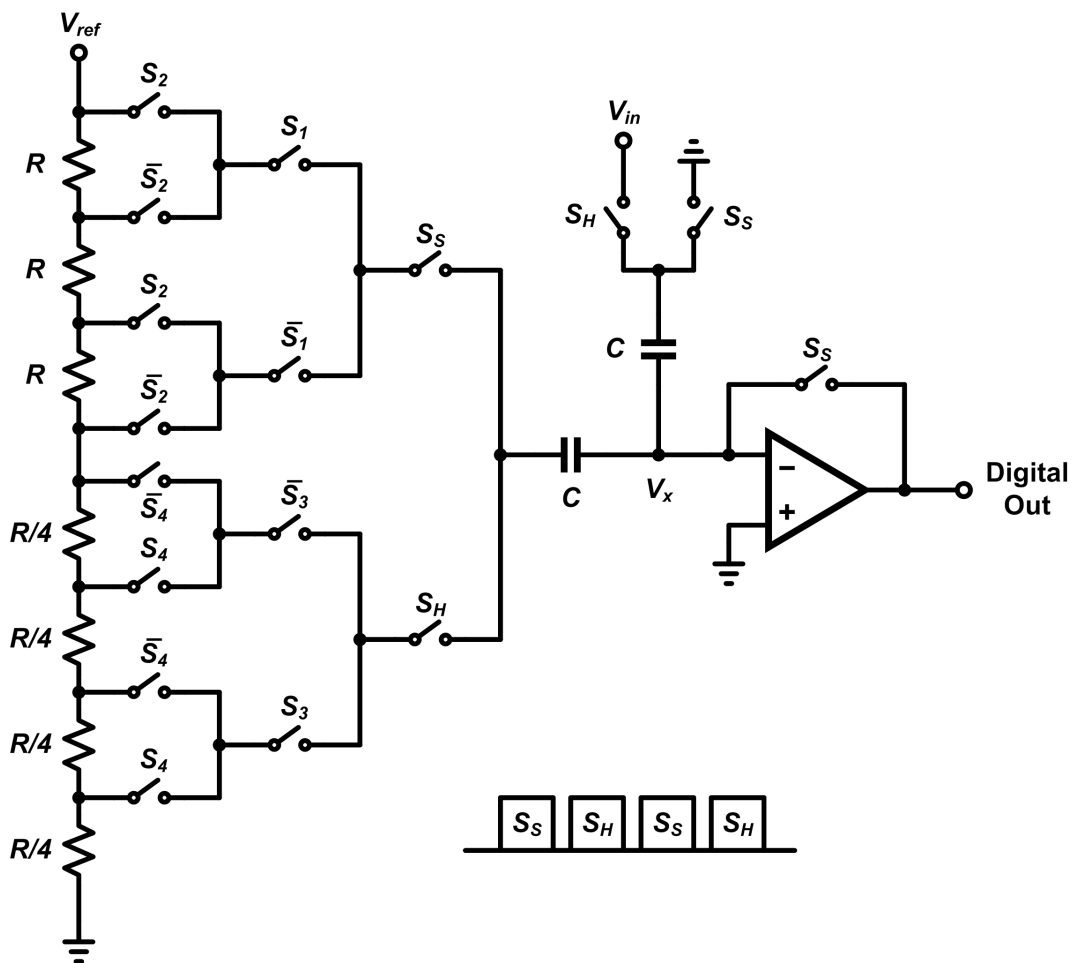
Midterm Examination

May 11, 2011, 3-3:50pm

1. In the binary-weighted 10-bit DAC shown on top, the capacitor array can be replaced as shown below.
 - a. Find the element values in the new DAC. Choose $C_6 = C_1$.
 - b. What are the advantages and disadvantages of the new circuit?



2. In the 4-bit SAR ADC shown, during the sampling phase the S_S switches are closed; during the next (hold) phase, the S_H switches are closed. After the hold phase, switches S_1 , S_2 , S_3 , and S_4 are used to test for the MSB, next MSB, etc.
- Which of these switches will be closed when the MSB is found?
 - Which switches are closed when the next bit is found if the MSB was 1?
 - Which switches are closed when the next bit is found if the MSB was 0?

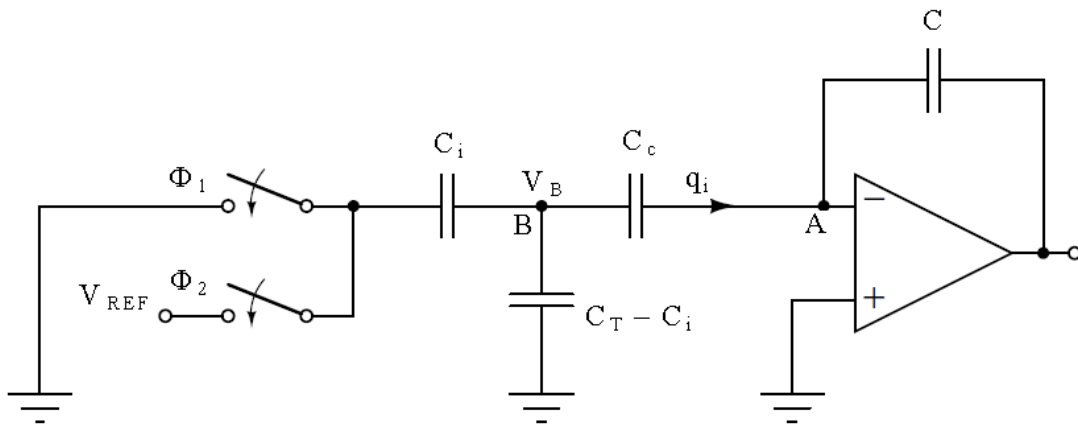


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Solution

1.

- a. Since $C_1, C_2 \dots C_5$ are connected in the same way as $\frac{C}{2}, \dots, \frac{C}{2^5}$ elements, and deliver $q_i = +C_i V_{ref}$ in to the virtual ground A,

$$C_i = 2^{-i}C, \text{ for } i = 1, 2, \dots, 5.$$



For $6 \leq i \leq 10$, we have

$$+q_i = C_c V_B = \frac{C_c C_i V_{REF}}{C_c + C_T} = \frac{C_i V_{REF}}{1 + \frac{C_T}{C_c}} \doteq \frac{C V_{REF}}{2^i} \text{ where}$$

$$C_T = \sum_{i=6}^{10} C_i$$

Since by assumption, $C_6 = C_1$, for $i = 6$,

$$\frac{C}{2} \frac{V_{REF}}{(1 + \frac{C_T}{C_c})} = \frac{C V_{REF}}{2^6}$$

$$\frac{C_T}{C_c} = 2^5 - 1 = 31$$

For $i = 7, 8, 9, 10$ therefore

$$\frac{C_i V_{REF}}{32} = \frac{C V_{REF}}{2^i}$$

$$C_i = 2^{5-i}C = C_{i-5}, C_7 = C_2, \dots$$

$$C_T = \sum_{i=1}^5 C_i = C \left(\frac{1}{2} + \frac{1}{4} + \dots + \frac{1}{32} \right) = \frac{31}{32}C$$

$$C_c = \frac{C_T}{31} = \frac{C}{32} = C_{10} = 32fF$$

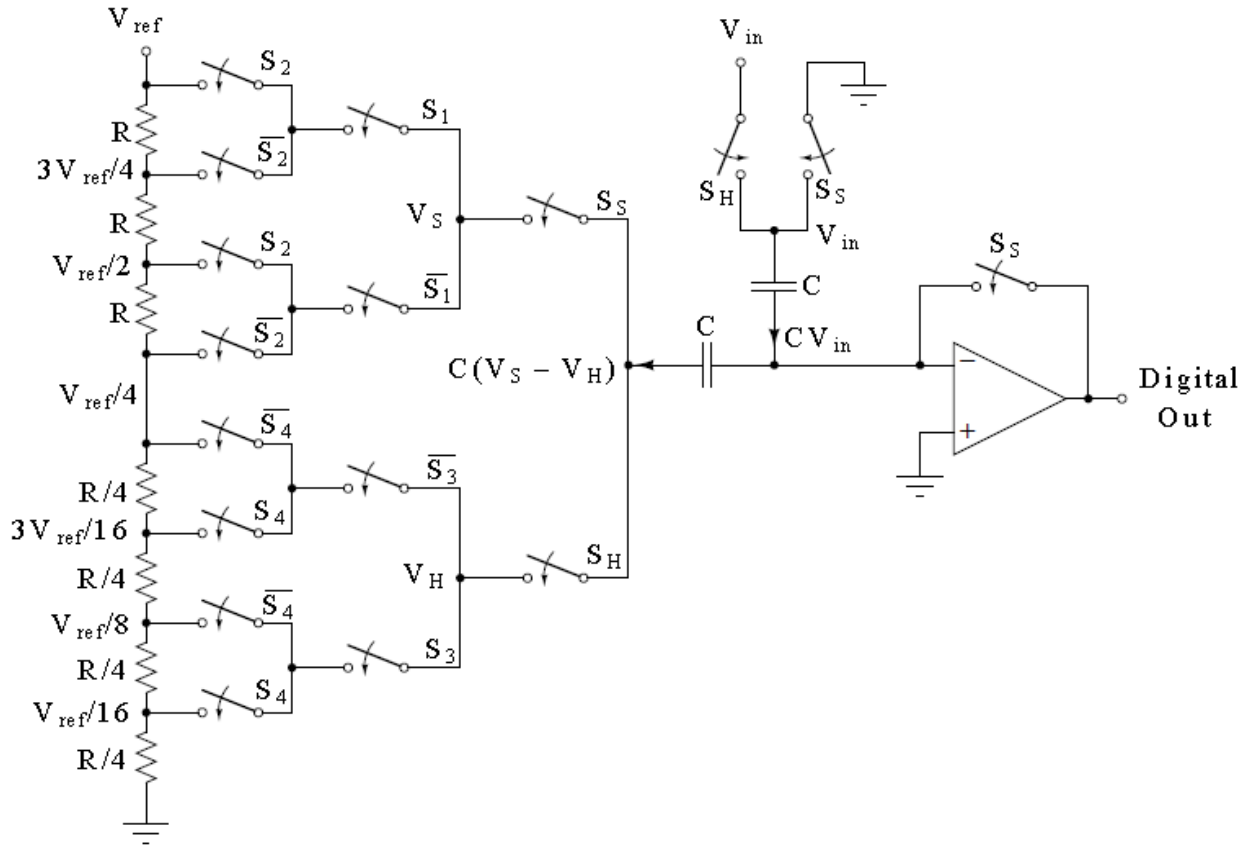
- b. The new circuit has one more capacitor. Spread of capacitors reduced by half, may be possible to scale all capacitors by $\frac{1}{2^5}$. Circuit is stray sensitive at left side terminal of C_c . Circuit is also sensitive to C_c . Monotonicity and glitch of the new circuit is possibly better. The new circuit is faster.

2. Charge flow through the capacitor in to $V_x = V_{os}$ as $S_H \rightarrow 1$.

$$q = CV_{in} - C(V_S - V_H)$$

- a. For MSB, $V_S - V_H \doteq \frac{V_{ref}}{2}$ obtained if $V_S = \frac{3}{4}V_{ref}$, $V_H = \frac{1}{4}V_{ref}$

$$S_1 = 1, S_2 = 0, S_3 = 0, S_4 = 0$$



b. If $MSB = 1$, next $V_S - V_H \doteq \frac{3}{4} V_{ref}$ obtained if $V_S = V_{ref}, V_H = \frac{1}{4} V_{ref}$

$$S_1 = 1, S_2 = 1, S_3 = 0, S_4 = 0$$

c. If $MSB = 0$, next $V_S - V_H \doteq \frac{1}{4} V_{ref}$ obtained if $V_S = \frac{V_{ref}}{2}, V_H = \frac{1}{4} V_{ref}$

$$S_1 = 0, S_2 = 1, S_3 = 0, S_4 = 0$$